REMARKS

This is in full and timely response to the Final Office Action mailed on February 13, 2004. Reexamination in light of the amendments and the following remarks is respectfully requested.

Claims 21-55 are currently pending in this application, with claims 21 and 39 being independent. No new matter has been added.

Rejections under 35 U.S.C. §112 and §103

While not conceding the propriety of this rejection and in order to advance the prosecution of this application, claims 2, 7-11, 13, and 15-20 have been canceled without prejudice or disclaimer of their underlying subject matter. Withdrawal of these rejections is respectfully requested.

Newly added claims

Claim 21 and the claims dependent thereon are drawn to a semiconductor package including the features of:

> a first insulating substrate having a first surface and a second surface opposite said first surface, said first surface having electrically conductive patterns and electrically conductive pattern lands formed thereon, said second surface having a heat dissipating pattern and second surface lands formed thereon;
>
> a heat radiating plate that radiates heat from within said semiconductor device, said heat dissipating pattern and said second surface lands being between said first insulating substrate and said heat radiating plate;

a semiconductor device bonded onto said first surface, bond wires connecting said semiconductor device to said electrically conductive patterns, said electrically conductive patterns being connected to said electrically conductive pattern lands;

a sidewall section on said first surface, said sidewall section encircling said semiconductor device, a cavity being a concave shape defined by said first insulating substrate and said sidewall section, said semiconductor device being contained within said cavity;

a second insulating substrate covering said sidewall section and said cavity, said second insulating substrate having a through-hole land portion and a solder land portion, said through-hole land portion being disposed at the rim of said second insulating substrate to contact said sidewall section, and a solder land portion being disposed at the central part of said second insulating substrate to contact said cavity;

through-hole lands disposed at said through-hole land portion;

solder lands disposed at said solder land portion;

conductor patterns connecting said solder lands to said through-hole lands; and

through-holes extending from said through-hole lands, through said second insulating substrate, said sidewall section, said electrically conductive pattern lands, said first surface, and said second surface, to said second surface lands, said through-holes being plated to form plated through-holes.

Claim 39 and the claims dependent thereon a method for the preparation of a semiconductor package comprising the steps of:

forming electrically conductive patterns and electrically conductive pattern lands on a first surface of a first insulating substrate;

forming a heat radiating plate that radiates heat from within said semiconductor device, said heat dissipating pattern and said second surface lands being between said first insulating substrate and said heat radiating plate;

bonding a semiconductor device onto said first surface;

connecting said semiconductor device to said electrically conductive patterns with bond wires;

connecting said electrically conductive patterns to said electrically conductive pattern lands;

encircling said semiconductor device with a sidewall section to form a cavity, said sidewall section being formed on said first surface, said cavity being a concave shape defined by said first insulating substrate and said sidewall section, said semiconductor device being contained within said cavity;

covering said sidewall section and said cavity with a second insulating substrate, said second insulating substrate having a through-hole land portion and a solder land portion, said through-hole land portion being disposed at the rim of said second insulating substrate to contact said sidewall section, and a solder land portion being disposed at the central part of said second insulating substrate to contact said cavity;

extending through-holes through said second insulating substrate, said sidewall section, said electrically conductive pattern lands, said first surface, and said second surface, to said second surface lands, said through-holes being plated to form plated through-holes;

forming through-hole lands at said through-hole land portion, said through-hole lands contacting said plated through-holes;

forming solder lands at said solder land portion; and

connecting said solder lands to said through-hole lands with conductor patterns.

Within the claims, a second insulating substrate covers the sidewall section and the cavity. The second insulating substrate has a through-hole land portion and a solder land portion. The through-hole land portion is disposed at the rim of the second insulating substrate to contact the sidewall section, and a solder land portion is disposed at the central part of the second insulating substrate to contact the cavity. Through-hole lands are disposed at the through-hole land portion, solder lands are disposed at the solder land portion, and conductor patterns connect the solder lands to the through-hole lands. These are absent from the related art described within the specification as originally filed and are absent from U.S. Patent No. 5,291,062 issued to Higgins, III (Higgins) at least for the following reasons.

The related art fails to disclose, teach or suggest a second insulating substrate that covers the sidewall section 74, 75 and the cavity 82 (figure 1). The Office Action admits that this feature is absent from the related art and cites Higgins for this deficient feature.

Higgins arguably teaches an area array semiconductor device having a lid with functional contacts. While figure 5 of Higgins arguably teaches conductive traces 85, it should be understood that the traces are not shorted together but are individual conductors (column 7, lines 5-7). Moreover, Higgins arguably teaches that an anisotropic conductive adhesive 90 electrically connects the plurality of conductive traces 85 on the lid 84 to the plurality of conductive traces 80 on the lid contact shelf 76 of substrate 72 (column 7, lines 16-19). Yet, Higgins fails to disclose, teach or suggest conductor patterns connecting the solder lands to the through-hole lands.

Within the claims, through-holes extend from the through-hole lands, through the second insulating substrate, the sidewall section, the electrically conductive pattern lands, the first surface, and the second surface, to the second surface lands, the through-holes being plated to form plated through-holes. These are absent from the related art described within the specification as originally filed and are absent from Higgins at least for the following reasons.

The related art fails to disclose, teach or suggest through-holes 91 extending through electrically conductive pattern lands. Instead, the related art arguably depicts through-holes 91 terminating at electrically conductive pattern lands (figure 1).

Higgins fails to disclose, teach or suggest through-holes extend from the through-hole lands, through the second insulating substrate, the sidewall section, the electrically conductive pattern lands, the first surface, and the second surface, to the second surface lands, the through-holes being plated to form plated through-holes.

Allowance of the claims is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753 or the undersigned attorney at the below-listed number.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

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Respectfully submitted,

By_____

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